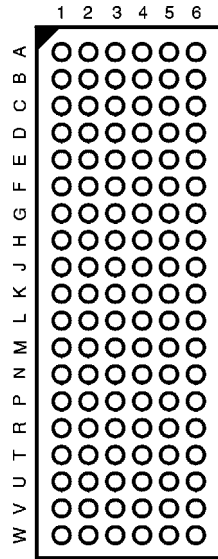


Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3, \overline{OE}_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B

FBGA Pin Assignments

(40-Bit Routing)

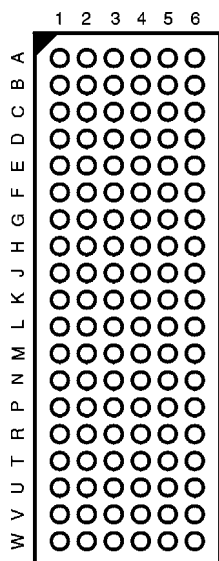
	1	2	3	4	5	6
A	1A ₂	1A ₁	NC	OE ₂	1B ₁	1B ₂
B	1A ₄	1A ₃	GND	OE ₁	1B ₃	1B ₄
C	1A ₆	1A ₅	GND	GND	1B ₅	1B ₆
D	1A ₈	1A ₇	GND	GND	1B ₇	1B ₈
E	1A ₁₀	1A ₉	V _{CC}	V _{CC}	1B ₉	1B ₁₀
F	2A ₂	2A ₁	V _{CC}	V _{CC}	2B ₁	2B ₂
G	2A ₄	2A ₃	V _{CC}	GND	2B ₃	2B ₄
H	2A ₆	2A ₅	GND	GND	2B ₅	2B ₆
J	2A ₈	2A ₇	2A ₉	2B ₉	2B ₇	2B ₈
K	2A ₁₀	3A ₁₀	GND	GND	3B ₁₀	2B ₁₀
L	3A ₉	3A ₈	GND	GND	3B ₈	3B ₉
M	3A ₇	3A ₆	GND	V _{CC}	3B ₆	3B ₇
N	3A ₅	3A ₄	V _{CC}	V _{CC}	3B ₄	3B ₅
P	3A ₃	3A ₂	V _{CC}	V _{CC}	3B ₂	3B ₃
R	3A ₁	4A ₁₀	GND	GND	4B ₁₀	3B ₁
T	4A ₉	4A ₈	GND	GND	4B ₈	4B ₉
U	4A ₇	4A ₆	GND	4B ₁	4B ₆	4B ₇
V	4A ₅	4A ₄	4A ₁	OE ₄	4B ₄	4B ₅
W	4A ₃	4A ₂	OE ₃	NC	4B ₂	4B ₃

Truth Tables

Inputs		Inputs/Outputs	
\overline{OE}_1	\overline{OE}_2	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Inputs		Inputs/Outputs	
\overline{OE}_3	\overline{OE}_4	3A, 3B	4A, 4B
L	L	3A = 3B	4A = 4B
L	H	3A = 3B	Z
H	L	Z	4A = 4B
H	H	Z	Z

Connection Diagram



(Top Thru View)

FBGA Pin Assignments

(48-Bit Routing)

	1	2	3	4	5	6
A	1A ₂	1A ₁	NC	OE ₂	1B ₁	1B ₂
B	1A ₄	1A ₃	1A ₇	OE ₁	1B ₃	1B ₄
C	1A ₆	1A ₅	GND	1B ₇	1B ₅	1B ₆
D	1A ₁₀	1A ₉	1A ₈	1B ₈	1B ₉	1B ₁₀
E	1A ₁₂	1A ₁₁	2A ₁	2B ₁	1B ₁₁	1B ₁₂
F	2A ₄	2A ₃	2A ₂	2B ₂	2B ₃	2B ₄
G	2A ₆	2A ₅	V _{CC}	GND	2B ₅	2B ₆
H	2A ₈	2A ₇	GND	GND	2B ₇	2B ₈
J	2A ₁₀	2A ₉	2A ₁₁	2B ₁₁	2B ₉	2B ₁₀
K	2A ₁₂	3A ₁₂	GND	GND	3B ₁₂	2B ₁₂
L	3A ₁₁	3A ₁₀	GND	GND	3B ₁₀	3B ₁₁
M	3A ₉	3A ₈	GND	V _{CC}	3B ₈	3B ₉
N	3A ₇	3A ₆	3A ₂	3B ₂	3B ₆	3B ₇
P	3A ₅	3A ₄	3A ₁	3B ₁	3B ₄	3B ₅
R	3A ₃	4A ₁₂	4A ₈	4B ₈	4B ₁₂	3B ₃
T	4A ₁₁	4A ₁₀	4A ₇	4B ₇	4B ₁₀	4B ₁₁
U	4A ₉	4A ₆	GND	4B ₁	4B ₆	4B ₉
V	4A ₅	4A ₄	4A ₁	OE ₄	4B ₄	4B ₅
W	4A ₃	4A ₂	OE ₃	NC	4B ₂	4B ₃

Pin Descriptions

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3, \overline{OE}_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B

Truth Tables

Inputs		Inputs/Outputs	
\overline{OE}_1	\overline{OE}_2	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Inputs		Inputs/Outputs	
\overline{OE}_3	\overline{OE}_4	3A, 3B	4A, 4B
L	L	3A = 3B	4A = 4B
L	H	3A = 3B	Z
H	L	Z	4A = 4B
H	H	Z	Z

Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	0.5V to +7.0V
DC Switch Voltage (V_S) (Note 4)	-0.5V to +7.0V
DC Input Control Pin Voltage (V_{IN}) (Note 5)	-0.5V to +7.0V
DC Input Diode Current (I_{IK}) $V_{IN} < 0V$	-50 mA
DC Output (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/- 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150 °C

Recommended Operating Conditions (Note 6)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40\text{ °C to }+85\text{ °C}$			Units	Conditions
			Min	Typ (Note 7)	Max		
V_{IK}	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18\text{ mA}$
V_{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
I_I	Input Leakage Current	5.5			± 1.0	μA	$0 \leq V_{IN} \leq 5.5V$
		0			10	μA	$V_{IN} = 5.5V$
I_{OZ}	OFF-STATE Leakage Current	5.5			± 1.0	μA	$0 \leq A, B \leq V_{CC}$
R_{ON}	Switch On Resistance (Note 8)	4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 64\text{ mA}$
		4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 30\text{ mA}$
		4.5		8	12	Ω	$V_{IN} = 2.4V, I_{IN} = 15\text{ mA}$
		4.0		11	20	Ω	$V_{IN} = 2.4V, I_{IN} = 15\text{ mA}$
I_{CC}	Quiescent Supply Current	5.5			3	μA	$OE_1 = OE_2 = GND$ $V_{IN} = V_{CC}$ or $GND, I_{OUT} = 0$
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One Input at 3.4V Other Inputs at V_{CC} or GND

Note 7: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25\text{ °C}$

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C},$ $C_L = 50\text{pF}, R_U = R_D = 500\Omega$				Units	Conditions	Figure Number
		$V_{CC} = 4.5 - 5.5\text{V}$		$V_{CC} = 4.0\text{V}$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus (Note 9)		0.25		0.25	ns	$V_I = \text{OPEN}$	Figures 1, 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	6.0		6.5	ns	$V_I = 7\text{V}$ for t_{PZL} $V_I = \text{OPEN}$ for t_{PZH}	Figures 1, 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	7.0		7.2	ns	$V_I = 7\text{V}$ for t_{PLZ} $V_I = \text{OPEN}$ for t_{PHZ}	Figures 1, 2

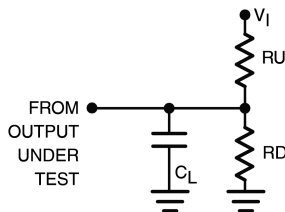
Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 10)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	$V_{CC} = 5.0\text{V}$
C_{IO}	Input/Output Capacitance	6		pF	$V_{CC}, \overline{OE} = 5.0\text{V}$

Note 10: $T_A = +25\text{ }^\circ\text{C}, f = 1\text{ MHz}$, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, $t_W = 500\text{ ns}$

FIGURE 1. AC Test Circuit

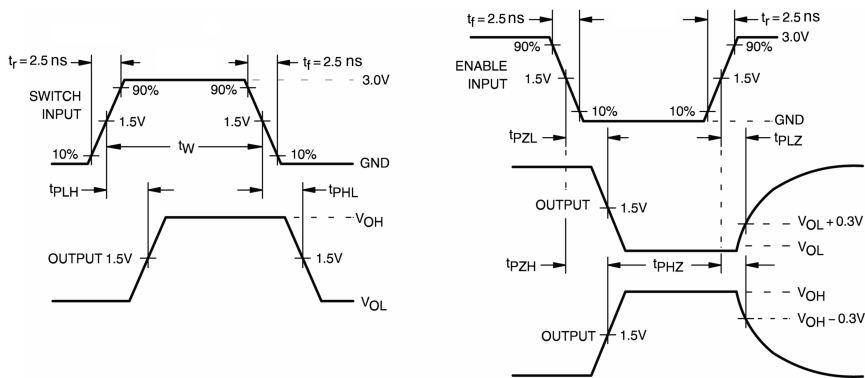
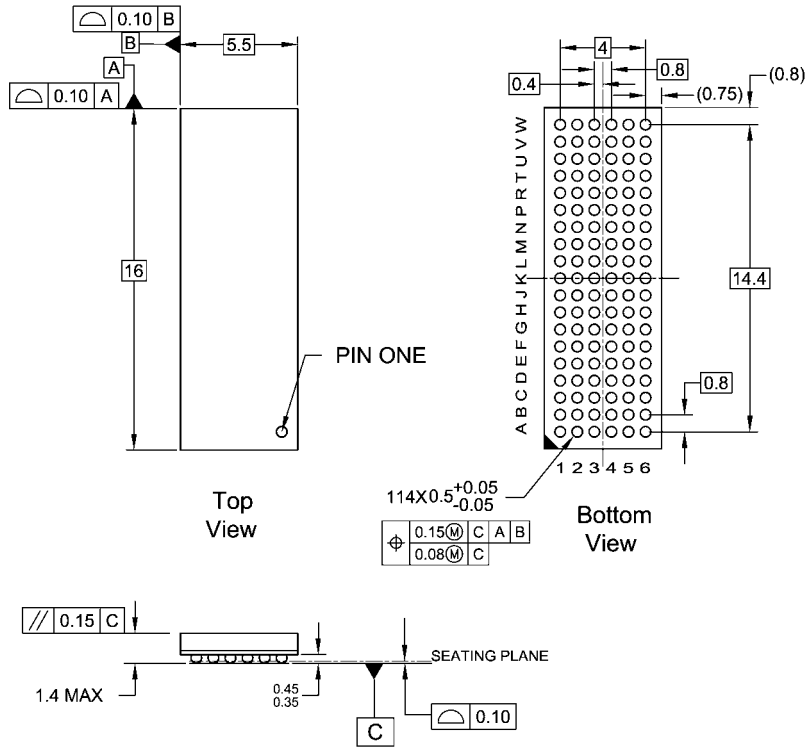


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
 - B. ALL DIMENSIONS IN MILLIMETERS
 - C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
 - D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

**114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A**

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com